

Code No: 126VN

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech III Year II Semester Examinations, February - 2023

VLSI DESIGN

(Electronics and Communication Engineering)

Time: 3 Hours

Max. Marks: 75

Note: i) Question paper consists of Part A, Part B.

ii) Part A is compulsory, which carries 25 marks. In Part A, Answer all questions.

iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A**(25 Marks)**

- 1.a) Define threshold voltage. [2]
- b) What is pass transistor and write its advantages. [3]
- c) Draw the layout diagram for NMOS inverter. [2]
- d) Compare stick and layout diagrams. [3]
- e) What are the different inverter delays? [2]
- f) Explain Domino Logic. [3]
- g) Compare the SRAM and DRAM. [2]
- h) Write the applications of parity circuits. [3]
- i) How the CPLD is different from FPGA. [2]
- j) Compare various simple PLDs. [3]

PART – B**(50 Marks)**

2. What are the different pull ups and explain their working with neat circuit diagram and also compare them. [10]

OR

- 3.a) Analyze the behaviour of CMOS inverter.
- b) Derive the value of Z_{pu}/Z_{pd} of inverter driven by another inverter. [5+5]

4. Explain the various steps involved in VLSI design flow in detail. [10]

OR

5. Draw the NMOS stick diagram for the following Boolean expression: $f = A + BC$. [10]

6. Describe about the choice of fan – in and fan – out selection in gate level design. [10]

OR

7. Design and explain the switch logic implementation for a four way multiplexer. [10]

8. Compare various memories in detail with architectures. [10]

OR

9. Design a 4-bit magnitude comparator and draw its layout. [10]

10. Explain the architecture of FPGA and what are the advantages of FPGA? [10]

OR

11. Explain chip level test techniques with techniques. [10]